H-300-08

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Y. OKAMOTO et al

Serial No. 09/922,656 Group Art Unit: 1756

Filed: August 7, 2001 Examiner: N. Barreca

For: PROCESS FOR FABRICATING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND EXPOSING SYSTEM AND MASK INSPECTING METHOD TO BE USED IN THE PROCESS

REPLY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 3, 2003

Sir:

In response to the Office Action dated August 1, 2003, please amend the above-identified application as follows. A petition and fee for a one-month extension of time accompany this response.